CLAIM AMENDMENTS

Please amend claims 1, 5, 8, 9, 13, 16, 18, and 20 as follows.

1. (Currently Amended) A timing circuit comprising:

at least one driving circuit outputting an output signal;

a phase locked loop receiving a reference clock signal and supplying an output clock signal to said at least one driving circuit, said phase locked loop generating said output clock signal according to said received reference clock signal and a feedback clock signal; and

first and second delay elements located in the path of said reference clock path and the path of said feedback clock path, respectively, said first and second delay elements to delay the feedback clock signal, to determine whether a rising edge of the delayed feedback clock signal is early or late with respect to a falling edge of the feedback clock signal, and to increase or decrease the delay of the feedback clock signal based on whether the rising edge of the delayed feedback clock signal is early or late with respect to the falling edge of the feedback clock signal ~~being configured to provide a delay in order to make said output signal meet a predetermined valid data timing requirement~~.

2. (Original) A timing circuit as claimed in claim 1, wherein delay elements are located only in the reference clock and feedback clock paths.

3. (Original) A timing circuit as claimed in claim 1, wherein said first and second delay elements are self-calibrating delay cells.

4. (Original) A timing circuit connection as claimed in claim 3, wherein said self-calibrating delay cells calibrate themselves to meet specified timing adjustment, granularity and/or range.

5. (Currently Amended) A timing circuit as claimed in claim 4, wherein said self-calibrating delay cells use a digital compensation technique to reduce process, voltage, and/or temperature (PVT) variations.

6. (Original) A timing circuit as claimed in claim 5, wherein said digital compensation technique utilizes a multi-tap delay buffer in the feedback clock signal path to delay the feedback clock signal, the amount of delay being controlled by selecting a tap of said multi-tap delay buffer.

7. (Original) A timing circuit as claimed in claim 1, wherein said at least one driving circuit comprises a plurality of driving circuits and said phase locked loop provides said output clock signal to all of said plurality of driving circuits.

8. (Currently Amended) A timing circuit as claimed in claim 7, wherein said plurality of driving circuits drive respective output signals from an integrated circuit (IC) chip.

9. (Currently Amended) An I/O circuit comprising:

a transmitting device outputting at least one output signal, said transmitting device having:

at least one driving circuit, the number of driving circuits corresponding to the number of output signals;

a phase locked loop receiving a reference clock signal and supplying an output clock signal to said at least one driving circuit, said phase locked loop generating said output clock signal according to said received reference clock signal and a feedback clock signal; and

first and second delay elements located in the path of said reference clock path and the path of said feedback clock, respectively, said first and second delay elements to delay the feedback clock signal, to determine whether a rising edge of the delayed feedback clock signal is early or late with respect to a falling edge of the feedback clock signal, and to increase or decrease the delay of the feedback clock signal based on whether the rising edge of the delayed feedback clock signal is early or late with respect to the falling edge of the feedback clock signal ~~being configured to provide a delay in order to make said output clock signal meet a predetermined valid data timing requirement~~; and

a receiving device receiving said at least one output signal from said transmitting device, the timing of said received at least one output signal meeting said predetermined valid timing requirement.

10. (Original) An I/O circuit as claimed in claim 9, wherein delay elements are located only in the reference clock and feedback clock paths.

11. (Original) An I/O circuit as claimed in claim 9, wherein said first and second delay elements are self-calibrating delay cells.

12. (Original) An I/O circuit as claimed in claim 11, wherein said self-calibrating delay cells calibrate themselves to meet specified timing adjustment, granularity and/or range.

13. (Currently Amended) An I/O circuit as claimed in claim 12, wherein said self-calibrating delay cells use a digital compensation technique to reduce process, voltage, and/or temperature (PVT) variations.

14. (Original) An I/O circuit as claimed in claim 13, wherein said digital compensation technique utilizes a multi-tap delay buffer in the feedback clock signal path to delay the feedback clock signal, the amount of delay being controlled by selecting a tap of said multi-tap delay buffer.

15. (Original) An I/O circuit as claimed in claim 9, wherein said at least one driving circuit comprises a plurality of driving circuits and said phase locked loop provides said output clock signal to all of said plurality of driving circuits.

16. (Currently Amended) An I/O circuit as claimed in claim 9, wherein said transmitting device and said receiving device comprise IC chips and said output signals are driven on a bus between said integrated circuit (IC) chips.

17. (Original) An I/O circuit as claimed in claim 16, wherein said transmitting device and said receiving device are mounted at a distance from each other on a printed circuit board.

18. (Currently Amended) A method of transferring a signal from a transmitting device to a receiving device comprising:

outputting said signal from said transmitting device using a driving circuit;

receiving a reference clock signal in said transmitting device;

generating an output clock signal according to said received reference clock signal and a feedback clock signal in a phase locked loop; and

providing a delay in a path of said reference clock signal and a path of said feedback clock signal, respectively, said delay phase-aligning a falling edge of the feedback clock signal to a rising edge of the delayed feedback clock signal ~~being configured~~ to make said at least one output signal meet a predetermined valid data timing requirement.

19. (Original) The method recited in claim 18, wherein said delay is provided by self-calibrating delay cells which calibrate themselves to meet specified timing adjustment, granularity and/or range.

20. (Currently Amended) The method recited in claim 19, wherein said self-calibrating delay cells use a digital compensation technique to reduce process, voltage, and/or temperature (PVT) variations.